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"What-If" Jitter Analysis from Synthesized Realistic PD Noise
Vishram Pandit (Intel Corp), Brian Wang (Intel Corp)

100 Gb/s Ethernet: Testing Receiver, Transmitter And Cable Assembly Parameters At Compliance Test Points
Chris Bridges (UNH-Io1), Christopher DiMinico (MC Communications/PHY-SI LLC), Curtis Donahue (University of New Hampshire Interoperability Test Lab), Oran Gafni (Intel), Mike Klempa (University of New Hampshire Interoperability Test Lab), Ken Ly (Cisco Systems), Adee Ran (Intel), Mike Resso (Keysight Technologies), Mike Sapozhnikov (Cisco Sytems)

100 Gb/s Serial Transmission Over Copper Using Duo-binary Signaling
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100Gbps Dual-Channel PAM4 Transmission Over Datacenter Interconnects
Sudeep Bhoja (Inphi), Frank Chang (Inphi), Karthik Gopalakrishman (Inphi), Sameer Herlekar (Inphi), Ishwar Hosagrahar (Inphi), Pulkit Khandelwal (Inphi Corporation), Jamal Riani (Inphi), Arun Tiruvur (Inphi), Jennifer Wu (Inphi)

25G Long Reach Cable Link System Equalization Optimization
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56 Gbps PCB Design Strategies for Clean, Low-Skew Channels
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A "Material" World, Modeling Dielectrics and Conductors for Interconnects Operating at 10-50 GBPS
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A Frequency Domain Approach to Transient Result for Power Distribution Network Analysis
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A New Characterization Technique for Glass Weave Skew Sensitivity
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A New SI-PI Co-Extraction Methodology & HSPICE Co-Simulation Simplification for A DDR3 Memory Interface
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A Novel Power-Supply-Induced-Jitter Suppression Technique for High-Speed Interface Using Modulated-PDN
Chia-Yu Chan (MediaTek), Shang-Pin Chen (MediaTek), Sheng-Feng Lee (MediaTek)

A Tutorial on PAM4 Signaling for 56G Serial Link Applications
Brandon Jiao (Xilinx), Yu Liao (Xilinx), Hongtao Zhang (Xilinx), Geoffrey Zhang (Xilinx)

A Versatile Spectrum Shaping Scheme for Communicating Beyond Notches in Multi-Drop Interfaces
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Accurate De-Embedding Using Differential Improved TRL
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Advanced PI and SI Co-Simulation Skills *Limited Seating
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An Introduction to MIPI SerDes Protocols
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Are There Any Rules of Thumb When It Comes to 100Gb/S Board Design? A Walkthrough From Physical Domain to Channel Operating Margin (COM) Testing
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Eugene Lim (Intel of Canada), Donald Telian (SI Guys Consulting)

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Yagnesh Waghela (Intel technology India PVT LTD)

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Deep Channel Analysis for 28 Gb/s and Beyond
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