



## Technical Papers

100 Gb/s Ethernet 100GBASE-CR4 Test Points and Test Fixtures

Christopher DiMinico (MC Communications), Mike Resso (Keysight Technologies), Mike Sapozhnikov (Cisco Systems)

56 Gb/s Serial Transmission using Duo-binary Signaling

Yu Ban (INTEC-IMEC), Johan Bauwelinck (Ghent University/iMinds), Jan De Geest (FCI), Timothy De Keulenaer (INTEC-IMEC), Bartek Kozicki (Alcatel-Lucent), Jeffrey Sinsky (Alcatel-Lucent), Guy Torfs (INTEC-IMEC)

A Brief Tour of FEC for Serial Link Systems

Shu Lin (University of California, Davis), Cathy Ye Liu (Avago Technologies), Michael Steinberger (Signal Integrity Software, Inc.)

A Cure for Intra-Pair Skew in High Speed Differential Signals      Michael Jenkins (Xilinx)

A Fast and Accurate Approach to Power Integrity Analysis for complex SiP

Ashish Gupta (Ericsson BMOD), Sheetal Jain (Ericsson BMOD), Taranjit Kukal (Cadence)

A Fast Method And Practical Considerations For Stable System Level Time-Domain Simulation Including DDR SSO Analysis

Sam Karikalan (Broadcom), Namhoon Kim (Broadcom), Uttara Sampath (Broadcom), Dharmendra Saraswat (Broadcom)

A New Methodology for Developing IBIS-AMI Models

Pegah Alavi (Keysight Technologies), John Baprawski (johnbaprawski.com), Hongtao Zhang (Xilinx), Geoff Zhang (Xilinx)

A Novel Approach to Model Dynamic Noise in Static Timing Analysis

Dan Oh (Altera), Yujeong Shim (Altera)

A Novel Method To Reduce Differential Crosstalk In A High-Speed Channel

Kunia Aihara (Hirose Electric USA), Jeremy Buan (Hirose Electric USA), Ching-Chao Huang (AtaiTec Corporation), Bill MacKillop (Hirose Electric USA), Toshiyuki Takada (Hirose Electric)

A Novel Simulation Flow to Expand Uses of IBIS-AMI Models in Mixed Tool Environment

YL Li (Intel Corp.), Weifeng Shu (Intel Asia Pacific Research & Development Ltd.), Xiaoning Ye (Intel Corp), Chunfei Ye (Intel Corp.), Xinjun Zhang (Intel Asia Pacific Research & Development Ltd.)

A Novel Stressed Eye Tolerance Test Methodology using IBIS AMI Modeling Techniques  
Venkatesh Avula (Seagate)

A Simple And Innovative Circuit Technique To Tackle Power Supply Induced Jitter In High Speed Serial Links For 25Gbps Transmission And Beyond  
Dan Oh (Altera Corporation), Yujeong Shim (Altera Corporation)

A Simple Method To Characterize And Accurately Remove The Effects Of Push-On Connectors  
Reiner Oppelt (Rosenberger Hochfrequenztechnik), Robert Schaefer (Keysight Technologies), Joachim Schubert (Rosenberger Hochfrequenztechnik)

A Systematic Merging and Isolation Strategy for I/O Power Integrity in Mobile Chipsets and Platforms  
Kai Chow (NVIDIA Corporation), Daehyun Chung (NVIDIA Corporation), Mona Fahim (NVIDIA Corporation), Daniel Lin (NVIDIA Corporation), Nithya Sankaran (NVIDIA Corporation), Sunil Sudhakaran (NVIDIA Corporation)

Accurate Statistical Analysis Of Serdes Links Considering Correlated Input Patterns, Data-Dependent Edge Transitions, And Transmit Jitter  
Vladimir Dmitriev Zdorov (Mentor Graphics)

Analytical Approaches for Worst and Statistical Eye Estimation in HBM Channel  
Kiyeong Kim (KAIST), Jinguok Kim (UNIST), Heegon Kim (KAIST), Hyungsoo Kim (SK Hynix), Jounggho Kim (KAIST), Jiseong Kim (KAIST)

Anisotropic Design Considerations for 28 Gbps Via to Stripline Transitions  
Scott McMorrow (Teraspeed Consulting - A Division of Samtec), Edward Sayre (Teraspeed Consulting, a division of Samtec Inc.)

At-Speed Testing of 32 Gbaud PAM-4 Interfaces using Automated Test Equipment  
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Augmenting Virtual Platform Simulations With Interface Electricals  
Todd Bermensolo (Intel Corporation), Dan Crain (Intel Corporation), Zao Liu (Intel), Peter Njenga (Intel Corporation)

Behavioral Model Of On-Die Voltage Regulator For Soc Power Delivery Analysis  
Jayong Koo (Intel), Xiaoping Liu (Intel Corporation), Ramnarayanan Muthukaruppan (Intel Corporation), Min Wang (Intel Corporation)

Behavioral Modeling of Random Jitter with Realistic Time and Frequency Dependence  
Scott Wedge (Synopsys, Inc.)

Behavioral RX Model Correlation with Physical Devices, and Accuracy Improvement  
Mike Peng Li (Altera), Timothy Lu (Altera), Masashi Shimanouchi (Altera), Hsinho Wu (Altera)

Breaking the 32 Gb/s Barrier: PCB Materials, Simulations, Measurements

Heidi Barnes (Keysight Technologies), Al Neves (Wild River Technology), Lee Ritchey (Speeding Edge),  
Tim Wang Lee (Wild River Technology)

Cascaded S-parameter or Combined 3DEM Modeling for DDR4 Memory Channel Design?

Hany Fahmy (Intelligent Solutions BVBA), Klaus Krohne (CST)

Causality Demystified

Chris Kocuba (Samtec), Jim Nadolny (Samtec), Stefaan Sercu (Samtec)

Characterization of PCB Insertion Loss with a New Calibration Method

Ning Cheng (Keysight Technologies), Gongxian Jia (Huawei Technologies), Faming Long (Huawei  
Technologies), Mike Resso (Keysight Technologies), Wenxue Zhu (Huawei)

Circuit, SI, PI Co-Design of LPDDR4 and LPDDR3

Isaac Ali (Intel Corp.), Ritochit Chakraborty (Intel Corp.), Ge Chang (Intel), Almarion F. Delos (Intel  
Corporation), Te-Yu (Jason) Kao (Intel Corp.), Vishram Pandit (Intel Corp), Ritesh B. Trivedi (Intel Corp.),  
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Co-Design for 1TB System Utilizing 33Gbps Transceivers in 20nm Technology

Ravindra Gali (Xilinx), Romi Mayder (Xilinx), Sarajuddin Niazi (Xilinx), Hong Shi (Xilinx)

Connectivity 2.0

Gary McCormack (Keyssa, Inc.)

Critical Memory Performance metrics for DDR4 systems

Barbara Aichinger (FuturePlus Systems)

DDR4 Board Design and Signal Integrity Verification Challenges

Nitin Bhagwath (Mentor Graphics Corporation), Chuck Ferry (Mentor Graphics Corporation), Motoaki  
Matsumura (Fujitsu Semiconductor Ltd.), Akihiro Miki (Fujitsu VLSI Ltd.), Arpad Muranyi (Mentor),  
Atsushi Sato (Fujitsu Semiconductor Ltd.), Randy Wolff (Micron Technology, Inc.)

Design and Characterization of a Low-Power, 6.4 Gbps Data Rate DDR Memory Interface System

Scott Best (Rambus Inc.), Michael Bucher (Rambus Inc.), Liji Gopalakrishnan (Rambus Inc.), Ravi Kollipara  
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Design and Characterization of Interconnects for Serial Links Operating at 56 Gbps and Beyond

Yeon-Chang Hahm (Rambus), Wendem Beyene (Rambus), Narayanan Mayandi (Rambus Inc.), Don  
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Design and Simulation of Equalizer Adaptation Engine in Multi-Protocol Serial Links  
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Design and Verification for High-Speed I/Os at Multiple to 60 Gbps With Jitter, Signal Integrity, and Power Optimization  
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Designing High Performance Interposers with 3-Port And 6-Port S-Parameters  
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Development of Low Transmission Loss Multi Wire Board  
Hiroyuki Yamaguchi (Hitachi Chemical Co.,Ltd.)

Does Skew Really Degrade SERDES Performance?  
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Effective Analysis Methodology for Reducing Power Management Integrated Circuit (PMIC) Coupling Noise in Mobile System Dongho Yu (Samsung Electronics)

Effective Roughness Dielectric To Represent Copper Foil Roughness In Printed Circuit Boards  
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Effects of Component Resonance on High-Speed Channel Performance  
Madhumitha Rengarajan (FCI USA LLC), Stephen Smith (FCI USA LLC), Andrew Zambell (FCI USA LLC)

Effects of Device Characteristics in Multi-Level Signaling Links  
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Efficient Analog and Mixed Signal Modeling using Digital Simulation Charles Geer (IBM)  
Electrodeposited Copper Foil Surface Characterization for Accurate Conductor Loss Modeling  
Michael Griesi (University of South Carolina)

Electromagnetic Noise Effects on Semiconductor System in Electric Vehicle  
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EMI Analysis of High-Speed I/O Connector in a Active System  
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Energy Proportional Power Management for Datacenter Applications  
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## Everything About S Parameters: Tips and Tricks for Correct Usage

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## Evolution of Transceiver Jitter and Noise Modeling in Behavioral Link Simulation

Mike Peng Li (Altera), Timothy Lu (Altera), Masashi Shimanouchi (Altera), Hsinho Wu (Altera)

## Extending the Reach of VCSEL Based 100 Gb/s Multimode Parallel Optic Links

Waruna Fernando (Avago Technologies), John Wilks (Avago Technologies)

## Fast Statistical Eye-Diagram Estimation For High-Speed Channel Including Receiver Circuit

Heegon Kim (KAIST), Kiyeong Kim (KAIST), Jingook Kim (UNIST), Hyungsoo Kim (SK Hynix), Jounggho Kim (KAIST), Changwook Yoon (Altera)

## Frequency-Dependent Input/Output Capacitance Of High Speed Serial IOs

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## Full-Wave Simulation vs. Multi-line S-Parameter Concatenation for Analysis at Frequencies up to 50 GHz

Stephen Smith (FCI USA LLC), Jeffrey Walden (EMC/SI RF, LLC)

## Getting Street-Smart about S Parameters

Richard Allred (Signal Integrity Software, Inc.), Peter LaFlamme (Signal Integrity Software, Inc.), Michael Mayer (Signal Integrity Software, Inc.), Michael Steinberger (Signal Integrity Software, Inc.), Todd Westerhoff (Signal Integrity Software, Inc.)

## High-Performance Enabling Parallel Buses for Exascale Systems

Gil Aguiar (NTK Technologies), Christian Baks (IBM Corporation), Noritaka Ban, Ph.D (NTK Technologies), Dr. Timothy Chainer, Ph.D (IBM Corporation), Michael Gaynes (IBM Corporation), Masakazu Hashimoto (Zeon Corporation), Dr. Manabu Hoshino, Ph.D (Zeon Corporation), Toshihiko Jimbo, Ph.D (Zeon Corporation), Junji Kodemura (Zeon Corporation), Atsushi Kuhara, Ph.D (NTK Technologies), Dr. Young Kwark, Ph.D (IBM Corporation), Aravind Nayak (Avago Technologies), Yoshiki Nukayam, Ph.D (NTK Technologies), Hajime Saiki, Ph.D (NTK Corporation), Lei Shan (IBM Corporation), Takuya Torii, Ph.D (NTK Technologies), Dr. Haitao (Tony) Xia (Avago Technologies)

## High-Speed Low-Power On-Chip Global Signaling Design Overview

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Josiah Bartlett (Tektronix), Sarah Boen (Tektronix), Ed Ford (Tektronix)

## IBIS-AMI Model Simulations over Six EDA Platforms

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IBIS-AMI Modeling and Simulation of 56G PAM4 Link Systems

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Impact of Regulator Sense-point Location on PDN Response

Joseph 'Abe' Hartman (Oracle), Kavitha Narayandass (Oracle), Istvan Novak (Oracle)

Impedance Measurement and Relating it to Control Loop Stability

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Jitter Failure Investigation Of High Speed Parallel Links In System On Chip Environment, Modeling And Mitigation Approach

Pratik Damle (STMicroelectronics), Rakesh Malik (STMicroelectronics), Jayanta Mukherjee (Indian Institute of Technology Bombay), Raj Kumar Nagpal (STMicroelectronics), Dr. Jai Narayan Tripathi (STMicroelectronics)

Method to Reduce Coupon Length for S-parameter Measurements

Shaowu Huang (Intel Corporation), Richard Kunze (Intel Corporation), Jeff Loyer (Intel Corporation), Boping Wu (Intel Corporation)

Minimization of Electromagnetic Interference Between PCB Antennas and Digital Interfaces

Mehdi Mechaik (IBM)

Mitigation of Fiber-Weave Effects by Broadside-Coupled Differential Striplines

Tomoyuki Akahoshi (Fujitsu Laboratories LTD.), Teng-Kai Chen (Molex), Taiga Fukumori (Fujitsu Laboratories Limited), Yasuo Hidaka (Fujitsu Laboratories of America, Inc.), Kenichi Kawai (Fujitsu Limited), Michael Lee (Fujitsu Laboratories of America, Inc.), Mark Lionbarger (Fujitsu Laboratories of America, Inc.), Daisuke Mizutani (Fujitsu Laboratories LTD.), Yasushi Mizutani (Fujitsu Limited), Hideaki Nagaoka (Fujitsu Laboratories Limited), Tetsuro Yamada (Fujitsu Advanced Technologies Limited), Takuji Yamamoto (Fujitsu Laboratories of America, Inc.)

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Moving Towards the Light, a Photonic Extensions API for OpenAccess

Susan Carver (Integration Initiative), Pieter Dumon (Luceda Photonics), Martin Fiers (Luceda Photonics), Kevin Nesmith (Silicon Integration Initiative)

My Product Failed EMI - Now What Do I Do?

Kenneth Wyatt (Wyatt Technical Services LLC)

Near-Field Magnetic Probe Method - Evanescent and Propagating Mode Measurements

Daniel Brooks (APREL Inc.)

New De-embedding Techniques for PCB Transmission-Line Characterization  
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New Metric Offers More Accurate Estimate Of Optical Transmitter's Impact On Multi-Mode Fiber-Optic Links

Greg D. Le Cheminant (Keysight Technologies), Piers Dawe (Mellanox Technologies), John Petrilla (Avago Technologies)

One-Sided Measurement of Power Supply Impedance Without Connectors  
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Optimization of PCB Capacitors for Signal Integrity Performance in Mixed Reference Channels  
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Optimizing Symmetry in Open Field Designs  
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Package Simulations For Mitigating Noise Coupling Onto Sensitive RF Signals  
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Passive 28G Precision ISI Channel to Assess DFE Effectiveness Empirically  
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PCB Layout Checking Methodology to Capture Power to I/O Coupling Issues  
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PCB Material and Copper Foil Considerations for Insertion Loss  
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PDN Modeling in the Presence of Multiple Power and "Ground" Pins  
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Power Delivery Noise and its Impact on Jitter and System Margin for Multi-Gb/s High-Speed Serial Interfaces  
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Power Measurements For EMI/EMC Testing  
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Power Referenced Design - How Bad is Not So Bad?  
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Topology Performance Comparison using eGaN FETs in 6.78 MHz Highly Resonant Wireless Power Transfer  
Michael de Rooij (Efficient Power Conversion), Johan Strydom (Efficient Power Conversion)

Ultrascale DDR4 De-Emphasis and CTLE Feature Optimization with Statistical Engine for BER Specification  
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Ultrascale FPGA DDR4 2400 Mbps System Level Design Optimization and Validation  
Dmitry Klokov (Xilinx), Wei Liu (Xilinx), Penglin Niu (Xilinx), Thomas To (Xilinx)

Understanding IBIS-AMI Simulations  
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Understanding the Effects of Channel Generated Skew on Chassis EMI  
Michael Fogg (FCI LLC USA)

Using Microprobing, Modeling and Error Correction Techniques to Optimize Channel Design"  
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Validation Of How Power/Ground Bump Reduction Decreases Average Power And Supply Noise  
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Vectorless Prediction of Simultaneous Switching Noise from FPGAs  
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What Makes a Good 25Gbps Channel? COM vs. BER Metrics  
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Wireless 101/201: Intro to RF & Microwave/Advanced Communication Systems Neil Jarvis (Rohde and Schwarz)